WHAT IS CLAIMED IS:

1. A method of forming a gate electrode of a multiple-gate transistor comprising:

providing a semiconductor structure including a semiconductor fin overlying an insulator layer, and a gate dielectric overlying at least a portion of the semiconductor fin;

forming a first gate electrode material overlying the gate dielectric;

forming a second gate electrode material overlying the first gate electrode material;

forming a patterned mask over the second gate electrode material;

etching the second gate electrode material; and

etching the first gate electrode material.

2. The method of claim 1 further comprising planarizing a non-planar top surface of the second gate electrode material to form a planarized top surface.

3. The method of claim 2 wherein the non-planar top surface is substantially conformal with respect to the semiconductor structure.

4. The method of claim 2 wherein planarizing a non-planar top surface comprises performing a chemical mechanical polishing process.

5. The method of claim 2 wherein the planarizing step exposes the first gate electrode material.

6. The method of claim 1 further comprising forming source and drain regions in the semiconductor fin.

7. The method of claim 1 further comprising:

forming spacers on the sides of the gate electrode;

performing selective epitaxy on the portions of the semiconductor fin not covered by the gate electrode; and

forming source and drain regions.

8. The method of claim 1 wherein the semiconductor fin comprises a silicon fin.

9. The method of claim 1 wherein the semiconductor fin comprises a silicon and germanium fin.

10. The method of claim 1 wherein the patterned mask comprises a mask material selected from a group comprising of silicon nitride, silicon oxynitride, silicon oxide, and photoresist, and combinations thereof.

11. The method of claim 1 wherein etching the second gate electrode material comprises performing a plasma etching process.

12. The method of claim 11 wherein the plasma etching process etches the second gate electrode material at a faster etch rate than it etches the first gate electrode material.

13. The method of claim 1 wherein the etching of the second gate electrode material stops on the first gate electrode material.

14. The method of claim 1 wherein etching the first gate electrode material comprises performing a plasma etching process or a wet etching process.

15. The method of claim 1 wherein the gate dielectric comprises silicon oxide.

16. The method of claim 1 wherein the gate dielectric comprises silicon oxynitride.

17. The method of claim 1 wherein the gate dielectric comprises a high permittivity material.

18. The method of claim 17 where the gate dielectric comprises a material selected from the group consisting of lanthanum oxide, aluminum oxide, hafnium oxide, hafnium oxynitride, and zirconium oxide, and combinations thereof.

19. The method of claim 17 wherein the gate dielectric comprises of high permittivity materials with relative permittivity greater than about 5.

20. The method of claim 1 wherein the gate dielectric has a thickness less than about 10 angstroms.

21. The method of claim 1 wherein the first gate electrode material is selected from a group comprising of poly-Si, poly-SiGe, a metallic nitride, a metallic silicide, or a metal, or combinations thereof.

22. The method of claim 1 wherein the second gate electrode material is selected from a group comprising of poly-Si, poly-SiGe, a metallic nitride, a metallic silicide, or a metal, or combinations thereof.

1 23. The method of claim 1 wherein the first gate electrode material comprises a metallic
2 nitride, and the second gate electrode material is selected from the group comprising of poly-Si,
3 poly-SiGe, a metallic nitride, a metallic silicide, and a metal.

1 24. The method of claim 1 wherein the first gate electrode material comprises a metal, and
2 the second gate electrode material is selected from a group comprising of poly-Si, poly-SiGe, a
3 metallic nitride, a metallic silicide, or a metal, or combinations thereof.

1 25. The method of claim 1 wherein the multiple-gate transistor is a triple-gate transistor.

1 26. The method of claim 1 wherein the multiple-gate transistor is a double-gate transistor.

27. A multiple-gate transistor structure comprising:

a semiconductor fin overlying an insulator layer;

a gate dielectric overlying at least a portion of the semiconductor fin;

a gate electrode overlying the gate dielectric, the gate electrode comprising a first gate electrode material underlying a second gate electrode material, wherein the first gate electrode material has a thickness of less than about 500 angstroms; and

source and drain regions in portions of the semiconductor fin oppositely adjacent to said gate electrode.

28. The structure of claim 27 wherein the first gate electrode material and the second gate electrode material are selected from a group consisting of poly-Si, poly-SiGe, a metallic nitride, a metallic silicide, and a metal, and combinations thereof.

29. The structure of claim 27 wherein the first gate electrode material comprises a metallic nitride, and the second gate electrode material is selected from a group consisting of poly-Si, poly-SiGe, a metallic nitride, a metallic silicide, and a metal, and combinations thereof.

30. The structure of claim 27 wherein the first gate electrode material comprises a metal, and the second gate electrode material is selected from a group consisting of poly-Si, poly-SiGe, a metallic nitride, a metallic silicide, and a metal, and combinations thereof.

31. The structure of claim 27 wherein the second gate electrode material has a substantially planar top surface.

32. The structure of claim 27 and further comprising spacers disposed on the sides of the gate electrode.

33. The structure of claim 27 wherein the semiconductor fin comprises silicon.

34. The structure of claim 27 wherein the semiconductor fin comprises silicon and germanium.

35. The structure of claim 27 wherein the semiconductor structure further comprises an etchant mask overlying the semiconductor fin.

36. The structure of claim 27 wherein the insulator layer is recessed, resulting in a notch at the base of the semiconductor fin.

37. The structure of claim 27 wherein the gate dielectric comprises silicon oxide.

38. The structure of claim 27 wherein the gate dielectric comprises silicon oxynitride.

39. The structure of claim 27 wherein the gate dielectric comprises a high permittivity material with relative permittivity greater than 5.

40. The structure of claim 39 wherein the gate dielectric comprises a material selected from the group consisting of lanthanum oxide, aluminum oxide, hafnium oxide, hafnium oxynitride, and zirconium oxide, and combinations thereof.

41. The structure of claim 27 wherein the gate dielectric has a thickness of less than about 10 angstroms.

1 42. The structure of claim 27 wherein the multiple-gate transistor is a triple-gate transistor.

1 43. The structure of claim 27 wherein the multiple-gate transistor is a double-gate transistor.

44. A method of forming semiconductor device, the method comprising:

providing a semiconductor-on-insulator substrate;

forming a semiconductor fin on the semiconductor-on-insulator substrate;

forming a gate dielectric over at least a portion of the semiconductor fin;

forming a first gate electrode material overlying the gate dielectric;

forming a second gate electrode material overlying the first gate electrode material;

planarizing the second gate electrode material;

etching the second gate electrode material selectively with respect to first gate electrode material; and

etching the first gate electrode material.

45. The method of claim 44 and further comprising forming source and drain regions in the semiconductor fin after etching the first gate electrode material.

46. The method of claim 45 and further comprising forming sidewall spacers along sidewalls of the semiconductor fin prior to forming source and drain regions.

47. The method of claim 44 wherein planarizing the second gate electrode material comprises performing a chemical mechanical polishing process.

48. The method of claim 47 wherein the planarizing step exposes the first gate electrode material.

49. The method of claim 44 wherein the gate dielectric comprises a high permittivity material with a relative permittivity greater than about 5.

50. The method of claim 44 wherein the first gate electrode material is selected from a group comprising of poly-Si, poly-SiGe, a metallic nitride, a metallic silicide, or a metal, or combinations thereof.

51. The method of claim 44 wherein the second gate electrode material is selected from a group comprising of poly-Si, poly-SiGe, a metallic nitride, a metallic silicide, or a metal, or combinations thereof.

52. The method of claim 51 wherein the first gate electrode material comprises a metallic nitride, and the second gate electrode material is selected from the group comprising of poly-Si, poly-SiGe, a metallic nitride, a metallic silicide, and a metal.

53. A method of forming a multiple gate transistor device, the method comprising:

providing a semiconductor structure including a semiconductor fin overlying an insulator layer, and a gate dielectric overlying at least a portion of the semiconductor fin;

forming a gate electrode material over the gate dielectric;

forming a planarizing layer over the gate electrode material;

etching the planarizing layer and the gate electrode material to form a gate electrode layer with a substantially planar upper surface; and

patterning and etching the gate electrode material to form a gate electrode.

54. The method of claim 53 wherein etching the planarizing layer and the gate electrode material comprises performing an etch back process.

55. The method of claim 53 wherein etching the planarizing layer and the gate electrode material comprises performing a chemical-mechanical polish process.

56. The method of claim 53 wherein the planarizing layer comprises a dielectric layer.

57. The method of claim 53 and further comprising forming a second gate electrode layer over the gate dielectric before forming the gate electrode material.

58. The method of claim 53 further comprising forming source and drain regions in the semiconductor fin.

59. The method of claim 53 further comprising:

forming spacers on the sides of the gate electrode;

performing selective epitaxy on the portions of the semiconductor fin not covered by the

gate electrode; and

forming source and drain regions.

60. The method of claim 53 wherein the semiconductor fin comprises a silicon fin.

61. The method of claim 53 wherein the semiconductor fin comprises a silicon and germanium fin.

62. The method of claim 53 wherein the gate dielectric comprises silicon oxide.

63. The method of claim 53 wherein the gate dielectric comprises silicon oxynitride.

64. The method of claim 53 wherein the gate dielectric comprises of high permittivity materials with relative permittivity greater than about 5.

65. The method of claim 64 where the gate dielectric comprises a material selected from the group consisting of lanthanum oxide, aluminum oxide, hafnium oxide, hafnium oxynitride, and zirconium oxide, and combinations thereof.

66. The method of claim 53 wherein the gate dielectric has a thickness less than about 10 angstroms.

67. The method of claim 53 wherein the first gate electrode material is selected from a group comprising of poly-Si, poly-SiGe, a metallic nitride, a metallic silicide, or a metal, or combinations thereof.

68. The method of claim 53 wherein the planarizing layer is formed from a material selected from the group consisting of silicon rich oxide, spin-on glass, silicon oxide, and doped glass.

69. The method of claim 53 wherein the planarizing layer comprises silicon rich oxide and the gate electrode material comprises polysilicon.